What is claimed is:

1. A semiconductor memory device comprising:

an oxide layer for isolating individual devices which define device areas so that a cell area and a peripheral circuit area are separated from each other on a semiconductor substrate;

a plurality of MOS transistors, comprising source areas, drain areas, and gates that are formed in the cell area and the peripheral circuit area;

a bit line, formed on the plurality of MOS transistors and electrically connected to the MOS transistor;

a stack-shaped capacitor, comprising a first electrode, a dielectric layer, and a second electrode, the bit line and the MOS transistors in the cell area being disposed beneath the stack-shaped capacitor;

a guard-ring pattern, interposed between the cell area and the peripheral circuit area, surrounding the cell area and being spaced apart from the peripheral circuit area; and

a contact fill for a plate electrode formed in the guard-ring pattern and in contact with the second electrode, the second electrode being formed on the internal sidewall and the bottom of the guard-ring pattern.

2. The device of claim 1, wherein the first electrode of the stack-shaped capacitor is electrically connected to the source areas and has a hollow cylindrical shape.

3. The device of claim 2, wherein the first electrode is conductive polycrystalline silicon (polysilicon).

4. The device of claim 3, wherein the first electrode further includes a barrier layer.

5. The device of claim 1, wherein the dielectric layer is formed of a high dielectric material.

6. The device of claim 5, wherein the high dielectric material is at least one selected from Ta_2O_5, PZT, PZLT, BST, and Al_2O_3.

7. The device of claim 1, wherein the second electrode is formed in block shape to overlap a predetermined region adjacent to the peripheral circuit area including the entire cell area.

8. The device of claim 7, wherein the second electrode is conductive polysilicon.

9. The device of claim 8, wherein the second electrode further includes a barrier layer.

10. The device of claim 1, wherein the guard-ring pattern is formed on a same surface as the bottom of the first electrode.

11. The device of claim 10, wherein the second electrode is extended to an edge of the cell area on a bottom of the guard-ring pattern.

12. The device of claim 1, wherein at least a part of the contact fill for the plate electrode is electrically connected to the second electrode in the guard-ring pattern.

13. The device of claim 1, wherein the contact fill for the plate electrode includes a tungsten fill that is formed of tungsten in the center, and barrier metal that is formed outside of the tungsten fill adjacent to a recessed portion.

14. The device of claim 13, wherein the barrier metal is a combination layer of Ti and TiN.

15. A method for manufacturing a semiconductor memory device, the method comprising:

a) separating a cell area from a peripheral circuit area on a semiconductor substrate and forming device active areas;

b) forming a plurality of MOS transistors in the device active areas of the cell area and the peripheral circuit area;

c) forming a first interlayer dielectric (ILD) film on the semiconductor substrate and forming a first electrode pattern and a guard-ring pattern surrounding the cell area on the first ILD film;

d) sequentially forming a conductive layer for a first electrode and an insulating layer for patterning on the first electrode pattern and the guard-ring pattern;

e) opening the entire cell area and a part of the guard-ring pattern, removing the conductive layer for the first electrode and the insulating layer for patterning to the first ILD film, and forming a first electrode node in the cell area;

f) removing the insulating layer for patterning that is filled in the first electrode node;

g) forming a dielectric layer and a conductive layer for a second electrode on the semiconductor substrate;

h) forming a pattern for a second electrode on the conductive layer for the second electrode; and

i) forming a contact fill for a plate electrode while being in contact with the second electrode that is formed on the sidewall and the bottom of the guard-ring pattern.

16. The method of claim 15, wherein the step a) includes the step of forming an insulating layer for isolating individual devices to define device active areas.

17. The method of claim 16, wherein the step of forming an insulating layer for isolating individual devices includes the steps of:

partially etching the semiconductor substrate to a predetermined depth and forming a trench; and

filling a silicon insulating layer in the trench.

18. The method of claim 15, wherein the step b) includes the steps of:

forming a gate in the device active areas;

forming source and drain junctions at both sides of the gate; and

forming a bit line on the gate.

19. The method of claim 18, wherein the step of forming a bit line includes the steps of:

forming a silicon insulating layer on the semiconductor substrate;

forming a bit line conductive layer and a mask insulating layer for self-alignment;

forming a bit line pattern on the bit line conductive layer and the mask insulating layer for self-alignment; and

forming an insulating layer spacer on the sidewall of the bit line pattern.

20. The method of claim 19, wherein the bit line conductive layer is a polycide layer in which conductive polysilicon is combined with a metal silicide layer.

21. The method of claim 19, wherein the mask insulating layer for self-alignment and the insulating layer spacer are formed of silicon nitride.

22. The method of claim 15, wherein the step c) includes the steps of:

forming a capacitor contact pad to be electrically connected to the MOS transistor;

thickly forming a first ILD film on the semiconductor substrate;

forming a photoresist on the first ILD film;

forming a first electrode pattern in the cell area in the photoresist and forming a band-shaped guard-ring pattern in a boundary between the cell area and the peripheral circuit area and surrounding the cell area; and

forming a first electrode pattern in the cell area on the first ILD film through dry etching using the patterned photoresist as a mask, and forming a guard-ring pattern in a boundary between the cell area and the peripheral circuit area while surrounding the cell area.

23. The method of claim 22, wherein the capacitor contact pad is formed by filling a conductive layer in a contact that is formed through self-alignment.

24. The method of claim 23, wherein the conductive layer is conductive polysilicon.

25. The method of claim 22, wherein the first ILD film includes a silicon nitride layer as an etch stopper in a lower portion of the first ILD film, and includes a silicon oxide layer that is formed on the etch stopper.

26. The method of claim 25, wherein the etch stopper is thinner than the silicon oxide layer.

27. The method of claim 15, wherein in the step d), the conductive layer for first electrode is conductive polysilicon.

28. The method of claim 27, wherein the conductive layer for the first electrode further includes a barrier layer.

29. The method of claim 28, wherein the barrier layer is one selected from TiN, RuO, Pt, Rb, and RbO.

30. The method of claim 15, wherein in the step d), the insulating layer for patterning is a silicon oxide layer that is formed through chemical vapor deposition (CVD).

31. The method of claim 15, wherein the step e) includes the steps of:

forming a photoresist on the insulating layer for patterning;

forming a cell opening pattern in the photoresist so that the peripheral circuit area is blocked and only the cell area is opened; and

sequentially etching and removing the second insulating layer and the conductive layer for the first electrode through dry etching using the cell opening pattern as a mask.

32. The method of claim 31, wherein the cell opening pattern is formed in the form of a block so that the cell opening pattern extends outside the cell area and at least partially overlaps the guard-ring pattern.

33. The method of claim 15, wherein the step f) includes the step of wet etching the insulating layer for patterning with etching solution.

34. The method of claim 33, wherein the etching solution is silicon oxide etchant containing hydrofluoric acid (HF) and buffered oxide etchant (BOE).

35. The method of claim 15, wherein the step g) includes the steps of:

forming a dielectric layer on the exposed surface of the first electrode node; and

forming a conductive layer for second electrode on the dielectric layer so that the inside of the first electrode node is filled.

36. The method of claim 35, wherein the dielectric layer is formed of at least one selected from silicon nitride, silicon oxide, and a high dielectric material.

37. The method of claim 36, wherein the high dielectric material is one selected from Ta_2O_5, Al_2O_3 and PZT, PLZT, and BST as perovskite-family ferroelectric materials.

38. The method of claim 35, wherein the conductive layer for the second electrode is conductive polysilicon.

39. The method of claim 38, wherein the conductive layer for the second electrode further includes a barrier layer.

40. The method of claim 15, wherein the step h) includes the steps of:

forming a photoresist on the conductive layer for second electrode;

forming a second electrode pattern having a block shape in the photoresist so that a part of the second electrode pattern overlaps partially the peripheral circuit area including the cell area and the guard-ring pattern; and

etching the conductive layer for second electrode, the dielectric layer and the conductive layer for first electrode remaining in the peripheral circuit area through dry etching using the patterned photoresist as a mask.

41.The method of claim 15, wherein the step i) includes the steps of:

forming a second ILD film on the entire surface of the semiconductor substrate;

forming a contact for plate electrode so that the sidewall and the bottom of the second electrode that is formed in the guard-ring pattern are exposed; and

forming a contact filling conductive layer in the contact for plate electrode so that the sidewall and the bottom of the second electrode are in contact with each other.

42. The method of claim 41, wherein the second ILD film is a silicon oxide layer that is formed through CVD.

43.The method of claim 41, wherein the step of forming a contact for the plate electrode includes the steps of:

forming a photoresist on the second ILD film;

forming a contact pattern for the plate electrode having a block shape in the photoresist to be larger than the actual size of the contact in an area where the photoresist overlaps the guard-ring pattern; and

dry etching and completely removing the second ILD film in the guard-ring pattern by using the patterned photoresist as a mask and forming a contact for the plate electrode so that the sidewall and the bottom of the second electrode in the guard-ring pattern are completely exposed.

44.The method of claim 41, wherein the step of forming a contact fill conductive layer in the contact for the plate electrode includes the steps of:

forming a contact filling conductive layer to be electrically connected to the second electrode on the semiconductor substrate; and

evenly removing the contact filling conductive layer to the second ILD film.

45. The method of claim 44, wherein the contact filling conductive layer is formed of tungsten (W).

46. The method of claim 45, wherein the contact filling conductive layer further includes Ti and TiN as a barrier layer.